

PTO/SB/08A (02-03)

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1

of 3

Complete if Known

Application Number	10/086,267
Filing Date	03/01/2002
First Named Inventor	Oscar E. Agazzi
Art Unit	2681
Examiner Name	n/a
Attorney Docket Number	BP 1904

U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

Examiner Initials ^a	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ^d
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
JAM		EP 1 006 697 A2	06-07-2000	Kameran Azadet		
JAM		EP 0 617 521 A2	09-28-1994	Zoran Kostic		

**Examiner
Signature**

Jacol Mehl

Date
Considered

9/30/05

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Sheet	2	of	3	Attorney Docket Number	BP 1904 Technology Center 2600

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
✓ JMW		W. Ellersick, C. K. Yang, M. Horowitz, and W. Dally, "GAD: A 12GS/s CMOS 4-bit A/D Converter for an Equalized Multi-Level Link," 1999 Symposium on VLSI Circuits, pp. 49-52.			
✓		W. Ellersick, C. K. Yang, V. Stojanovic, S. Modjtahedi, and M. A. Horowitz, "A Serial-Link Transceiver Based on 8Gsample/s A/D and D/A Converters in 0.25 um CMOS," 2001 IEEE International Solid-State Circuits Conference, San Francisco, February 2001, 3 pages.			
✓		C. K. Yang, V. Stojanovic, S. Modjtahedi, M. A. Horowitz, and W. F. Ellersick, "A Serial-Link Transceiver Based on 8Gsample/s A/D and D/A Converters in 0.25 um CMOS," IEEE Journal of Solid-State Circuits, Vol.36, No.11, November 2001, pp. 1684-1692.			
✓		C. S. G. Conroy, D. W. Cline, and P. R. Gray, "An 8-b 85MS/s Parallel Pipeline AID Converter in 1 um CMOS," IEEE Journal of Solid-State Circuits, Vol.28, No.4, April 1993, pp. 447-454.			
✓		J-E. Eklund and F. Gustafsson, "Digital Offset Compensation of Time-Interleaved ADC Using Random Chopper Sampling," International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland, pp. III-447-III-450.			
✓		Y-C. Jenq, "Digital Spectra of Nonuniformly Sampled Signals: A Robust Sampling Time Offset Estimation Algorithm for Ultra High-Speed Waveform Digitizers Using Interleaving," IEEE Transactions on Instrumentation and Measurements, Vol.39, No.1, February 1990, pp. 71-75.			
✓		D. Fu, K. C. Dyer, S. H. Lewis, and P. J. Hurst, "A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters," IEEE Journal of Solid-State Circuits, Vol.33, No.12, December 1998, pp. 1904-1911.			
✓		C. K. Yang, "Design Techniques for High-Speed Chip-to-Chip Links," http://web.doe.carleton.ca/courses/97578/topic5/Tutorial_SerialLink.pdf , 31 pages.			
✓		W. J. Dally and J. Poultion, "Transmitter Equalization for 4Gb/s Signalling," Proceedings of Hot Interconnects IV, Palo Alto, 1996, 10 pages.			
✓		W. C. Black and D. A. Hodges, "Time Interleaved Converter Arrays," IEEE Journal of Solid-State Circuits, Vol. SC-15, No.6, December 1980, pp. 1022-1029.			

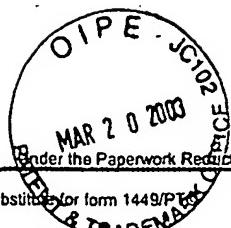
Examiner Signature	Jarod Meek	Date Considered	9/30/05
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OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS

Examiner Signature	<i>Jarol Green</i>	Date Considered	9/30/05
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